IN THE DRAWINGS:

Enclosed are new formal drawings of Figures 1 and 3, accompanied by a Letter to the Official Draftsperson. Figures 1 and 3 have been amended as illustrated in red on the attached photocopies. The new formal drawings include the noted changes.

REMARKS

Claim Rejections

Claims 1-5, 10, 11, 14-17, 19-20 and 23-24 are rejected under 35 U.S.C. § 102(b) as being anticipated by Giri et al. (U.S. 6,765,152). Claims 6, 7, 12, and 20-21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. in view of Klein et al. (U.S. 2004/0145051). Claim 8 is rejected under 35 U.S.C. §103(a) as being unpatentable over Giri et al. in view of Kikuma et al. (U.S. 6,621,169). Claims 9 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. in view of Koopmans (U.S. 2004/0035840). Claims 13 and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. in view of Higgins III (U.S. 5,583,377).

Drawings

The Examiner has objected to the drawings under 37 C.F.R. § 1.84(p)(4) insofar as reference numbers "113" and "140" have been used to designate the same thing. Individual reference lines have been added so that reference number 113 indicates the opening and reference number 140 indicates the packaging body. No "new matter" has been added to the original disclosure by the proposed amendments to these figures. It is believed the foregoing amendments obviate the outstanding objections to the drawings.

Applicant has enclosed formal drawings of Figures 1 and 3 accompanied by a Letter to the Official Draftsperson. The new formal drawings include the proposed changes. Entry of the corrected drawings is respectfully requested.

The Examiner has objected to the drawings under 37 C.F.R. § 1.84(p)(4) insofar as reference character "130" has been used to designate both the dummy die and package. Applicant respectfully notes that reference number "130" in Figure 2 is illustrating the dummy die and not the flip-chip package. Therefore, Applicant believes that no drawing corrections are necessary.

New Claims

By this Amendment, Applicant has canceled claims 1-24 and has added new claims 25-38 to this application. It is believed that the new claims specifically set forth each element of Applicant's invention in full compliance with 35 U.S.C. § 112, and define subject matter that is patentably distinguishable over the cited prior art, taken individually or in combination.

The new claims are directed toward a flip-chip package comprising: a substrate (110) having: a top substrate surface (111); a bottom substrate surface (112); a substrate opening (113) extending through the top surface and the bottom surface, the substrate opening includes a stair (114) located on an interior circumference thereof; and a plurality of solder balls (150) connected to the bottom substrate surface; a dummy die (130) connected to the bottom substrate surface and aligned with the substrate opening having a redistribution layer (133), the redistribution layer having a plurality of flip-chip pads (134) and a plurality of connecting pads (135) connected by an integrated circuit trace (136), the plurality of flip-chip pads and the plurality of connecting pads are located on a top surface of the dummy die below the stair of the substrate opening, the plurality of connecting pads of the redistribution layer are electrically connected to the substrate; and a chip (120) located in the opening and having a plurality of bumps (121) electrically connected to the plurality of flip-chip pads of the redistribution layer.

Other embodiments of the present invention include: a package body (140) located in the substrate opening and encasing the chip; the substrate is a printed circuit board; the dummy die has a size larger than a size of the chip; each of the plurality of flip-chip pads have a pitch smaller that a pitch of each of the plurality of connecting pads; each of the plurality of flip-chip pads have a pitch less than 150 μm; a plurality of bonding wires (137) electrically connecting the plurality of connecting pads to the substrate; a plurality of bumps (232) electrically connecting the plurality of connecting pads to the substrate; a plurality of top connection pads (116) located on the top substrate surface; the plurality of top connection pads of a top flip-chip package are connected to the plurality of bottom solder balls of a bottom top flip-chip package; and an adhesive tape (115) connecting the dummy die to the bottom substrate surface; the dummy die has an exposed surface (132) located on

a bottom thereof, the exposed surface has a metal thermal-conducting layer (233) formed thereon.

The primary reference to Giri et al. discloses a multi-chip module having chips on two sides including a frame (12), a large semiconductor device (22), a thin-film structure (18), and a plurality of semiconductor devices (20) located below the thin-film structure. The thin-film structure of Giri et al. should not be considered a dummy die.

In the present invention, the dummy die 130 with RDL 133 is a semiconductor substrate without active components, which provides a tough structure for mounting a flip chip 120 and connecting bonding wires 137, also provides a zero stress between the flip chip 120 and the dummy die 130.

Giri et al. do not teach the substrate opening includes a stair located on an interior circumference thereof; the plurality of flip-chip pads and the plurality of connecting pads are located on a top surface of the dummy die below the substrate opening; a package body located in the substrate opening and encasing the chip; each of the plurality of flip-chip pads have a pitch smaller that a pitch of each of the plurality of connecting pads; each of the plurality of flip-chip pads have a pitch less than 150 μm; a plurality of bonding wires electrically connecting the plurality of connecting pads to the substrate; a plurality of bumps electrically connecting the plurality of connecting pads to the substrate; the plurality of top connection pads of a top flip-chip package are connected to the plurality of bottom solder balls of a bottom top flip-chip package; each of the plurality of flip-chip pads have a pitch less than 150 μm; an adhesive tape connecting the dummy die to the bottom substrate surface; nor do Giri et al. teach the dummy die has an exposed surface located on a bottom thereof, the exposed surface has a metal thermal-conducting layer formed thereon.

It is axiomatic in U.S. patent law that, in order for a reference to anticipate a claimed structure, it must clearly disclose each and every feature of the claimed structure. Applicant submits that it is abundantly clear, as discussed above, that Giri et al. do not disclose each and every feature of Applicant's new claims and, therefore, could not possibly anticipate these claims under 35 U.S.C. § 102. Absent

a specific showing of these features, Giri et al. cannot be said to anticipate any of Applicant's new claims under 35 U.S.C. § 102.

The secondary reference to Klein et al. discloses a semiconductor component having a stacked dice and including a base die (12) a first secondary die (14-1) a second secondary die (14-2), terminal contacts (18) and a package substrate (120). There is no indication that either of the first secondary or the second secondary die is a chip.

Klein et al. do not teach the substrate opening includes a stair located on an interior circumference thereof; a substrate having a plurality of solder balls connected to the bottom substrate surface; the plurality of flip-chip pads and the plurality of connecting pads are located on a top surface of the dummy die below the substrate opening; a chip located in the opening and having a plurality of bumps electrically connected to the plurality of flip-chip pads of the redistribution layer; each of the plurality of flip-chip pads have a pitch less than 150 μm; an adhesive tape connecting the dummy die to the bottom substrate surface; nor do Klein et al. teach the dummy die has an exposed surface located on a bottom thereof, the exposed surface has a metal thermal-conducting layer formed thereon.

The secondary reference to Kikuma et al. discloses a stacked semiconductor device including a substrate (108), a semiconductor chip (102) located on the substrate and having a redistribution layer (114), a chip (104) located above the redistribution layer, bonding wires (116) connecting the distribution layer to the substrate, and an adhesive (112) connecting the semiconductor chip to the substrate.

Kikuma et al. do not teach the plurality of flip-chip pads and the plurality of connecting pads are located on a top surface of the dummy die below the substrate opening; a chip located in the opening and having a plurality of bumps electrically connected to the plurality of flip-chip pads of the redistribution layer; a substrate having a substrate opening extending through the top surface and the bottom surface; the substrate opening includes a stair located on an interior circumference thereof; each of the plurality of flip-chip pads have a pitch less than 150 μm; an adhesive tape connecting the dummy die to the bottom substrate surface; nor do

Kikuma et al. teach the dummy die has an exposed surface located on a bottom thereof, the exposed surface has a metal thermal-conducting layer formed thereon.

The secondary reference to Koopmans discloses a component installation removal and replacement apparatus including a substrate (34), connected to contacts (26, 28) by a redistribution layer (21), the redistribution layer is located on a flip-chip (10) and includes first and second dielectric layers (22, 24).

Koopmans does not teach a substrate having a substrate opening extending through the top surface and the bottom surface; the substrate opening includes a stair located on an interior circumference thereof; a dummy die connected to the bottom substrate surface and aligned with the substrate opening having a redistribution layer; the redistribution layer having a plurality of flip-chip pads and a plurality of connecting pads connected by an integrated circuit trace; the plurality of flip-chip pads and the plurality of connecting pads are located on a top surface of the dummy die below the substrate opening; each of the plurality of flip-chip pads have a pitch less than 150 μm; an adhesive tape connecting the dummy die to the bottom substrate surface; nor does Koopmans teach the dummy die has an exposed surface located on a bottom thereof, the exposed surface has a metal thermal-conducting layer formed thereon.

The secondary reference to Higgins, III teaches a pad array semiconductor device including a substrate (42) with an opening (20) having a ledge (44), a heat sink (46) located in an opening, and a semiconductor die (13) located on the heat sink .

Higgins, III does not teach a dummy die connected to the bottom substrate surface and aligned with the substrate opening having a redistribution layer; the redistribution layer having a plurality of flip-chip pads and a plurality of connecting pads connected by an integrated circuit trace; the plurality of flip-chip pads and the plurality of connecting pads are located on a top surface of the dummy die below the substrate opening; each of the plurality of flip-chip pads have a pitch less than 150 μm; an adhesive tape connecting the dummy die to the bottom substrate surface; nor does Higgins, III teach the dummy die has an exposed surface located on a bottom thereof, the exposed surface has a metal thermal-conducting layer formed thereon.

Even if the teachings of Giri et al., Klein et al., Kikuma et al., Koopmans, and Higgins, III were combined, as suggested by the Examiner, the resultant combination does not suggest: the plurality of flip-chip pads and the plurality of connecting pads are located on a top surface of the dummy die below the substrate opening; each of the plurality of flip-chip pads have a pitch less than 150 μm; an adhesive tape connecting the dummy die to the bottom substrate surface; nor does the combination suggest the dummy die has an exposed surface located on a bottom thereof, the exposed surface has a metal thermal-conducting layer formed thereon.

It is a basic principle of U.S. patent law that it is improper to arbitrarily pick and choose prior art patents and combine selected portions of the selected patents on the basis of Applicant's disclosure to create a hypothetical combination which allegedly renders a claim obvious, unless there is some direction in the selected prior art patents to combine the selected teachings in a manner so as to negate the patentability of the claimed subject matter. This principle was enunciated over 40 years ago by the Court of Customs and Patent Appeals in In re Rothermel and Waddell, 125 USPQ 328 (CCPA 1960) wherein the court stated, at page 331:

> The examiner and the board in rejecting the appealed claims did so by what appears to us to be a piecemeal reconstruction of the prior art patents in the light of appellants' disclosure. ... It is easy now to attribute to this prior art the knowledge which was first made available by appellants and then to assume that it would have been obvious to one having the ordinary skill in the art to make these suggested reconstructions. While such a reconstruction of the art may be an alluring way to rationalize a rejection of the claims, it is not the type of rejection which the statute authorizes.

The same conclusion was later reached by the Court of Appeals for the Federal Circuit in Orthopedic Equipment Company Inc. v. United States, 217 USPQ 193 (Fed.Cir. 1983). In that decision, the court stated, at page 199:

> As has been previously explained, the available art shows each of the elements of the claims in suit. Armed with this information, would it then be

> non-obvious to this person of ordinary skill in the art to coordinate these elements in the same manner as the claims in suit? The difficulty which attaches to all honest attempts to answer this question can be attributed to the strong temptation to rely on hindsight while undertaking this evaluation. It is wrong to use the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims in suit. Monday morning quarterbacking is quite improper when resolving the question of non-obviousness in a court of law.

In In re Geiger, 2 USPQ2d, 1276 (Fed.Cir. 1987) the court stated, at page 1278:

> We agree with appellant that the PTO has failed to establish a *prima facie* case of obviousness. Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching suggestion or incentive supporting the combination.

Applicant submits that there is not the slightest suggestion in either Giri et al., Klein et al., Kikuma et al., Koopmans, or Higgins, III that their respective teachings may be combined as suggested by the Examiner. Case law is clear that, absent any such teaching or suggestion in the prior art, such a combination cannot be made under 35 U.S.C. § 103.

Neither Giri et al., Klein et al., Kikuma et al., Koopmans, nor Higgins, III disclose, or suggest a modification of their specifically disclosed structures that would lead one having ordinary skill in the art to arrive at Applicant's claimed structure. Applicant hereby respectfully submits that no combination of the cited prior art renders obvious Applicant's new claims.

Summary

In view of the foregoing amendments and remarks, Applicant submits that this application is now in condition for allowance and such action is respectfully requested. Should any points remain in issue, which the Examiner feels could best be resolved by either a personal or a telephone interview, it is urged that Applicant's local attorney be contacted at the exchange listed below.

Respectfully submitted,

Date: December 20, 2004 By: 

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ANNOTATED MARKED-UP DRAWING

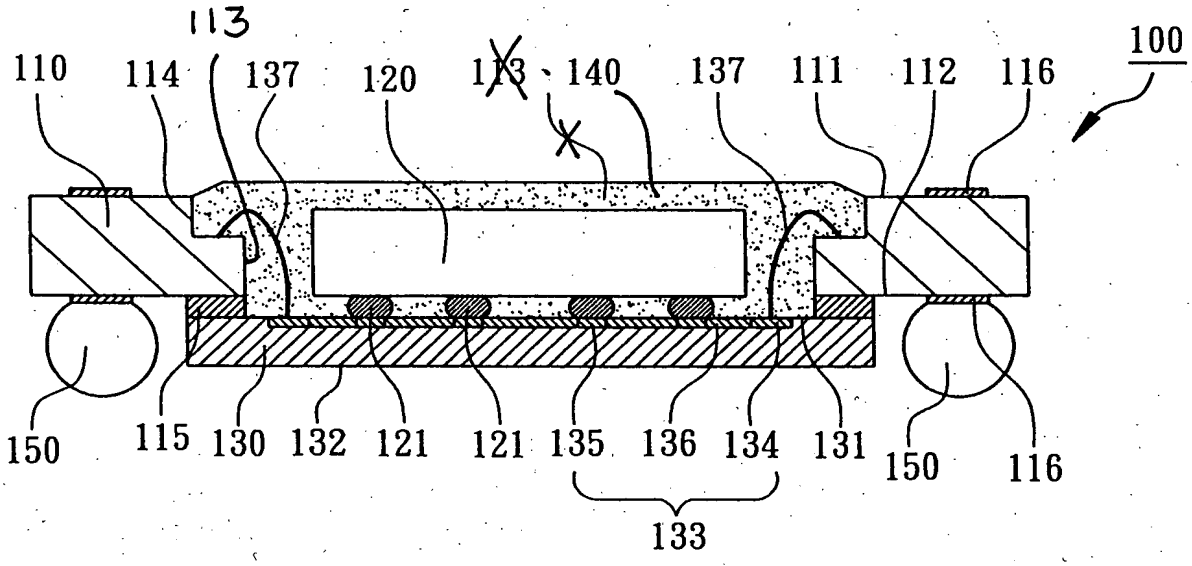

FIG. 1

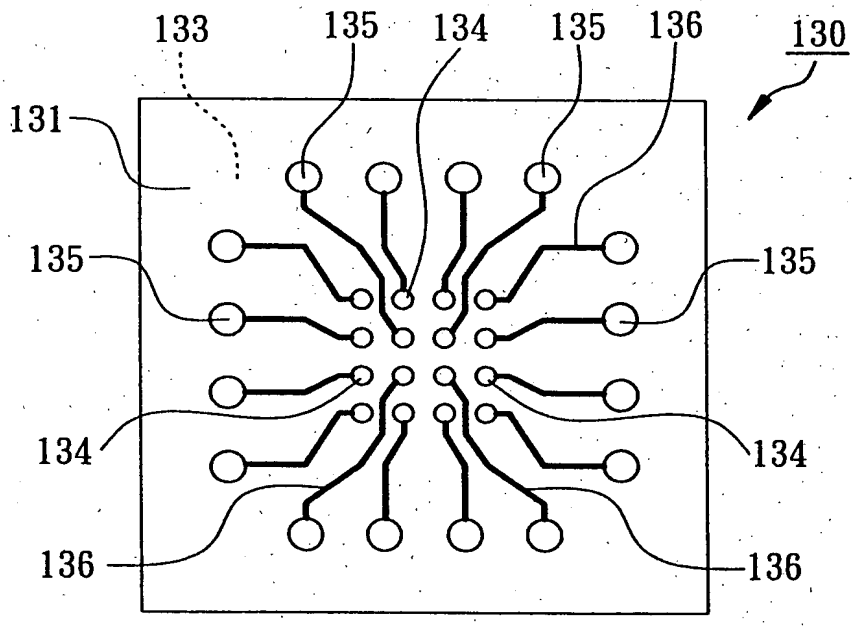

FIG. 2

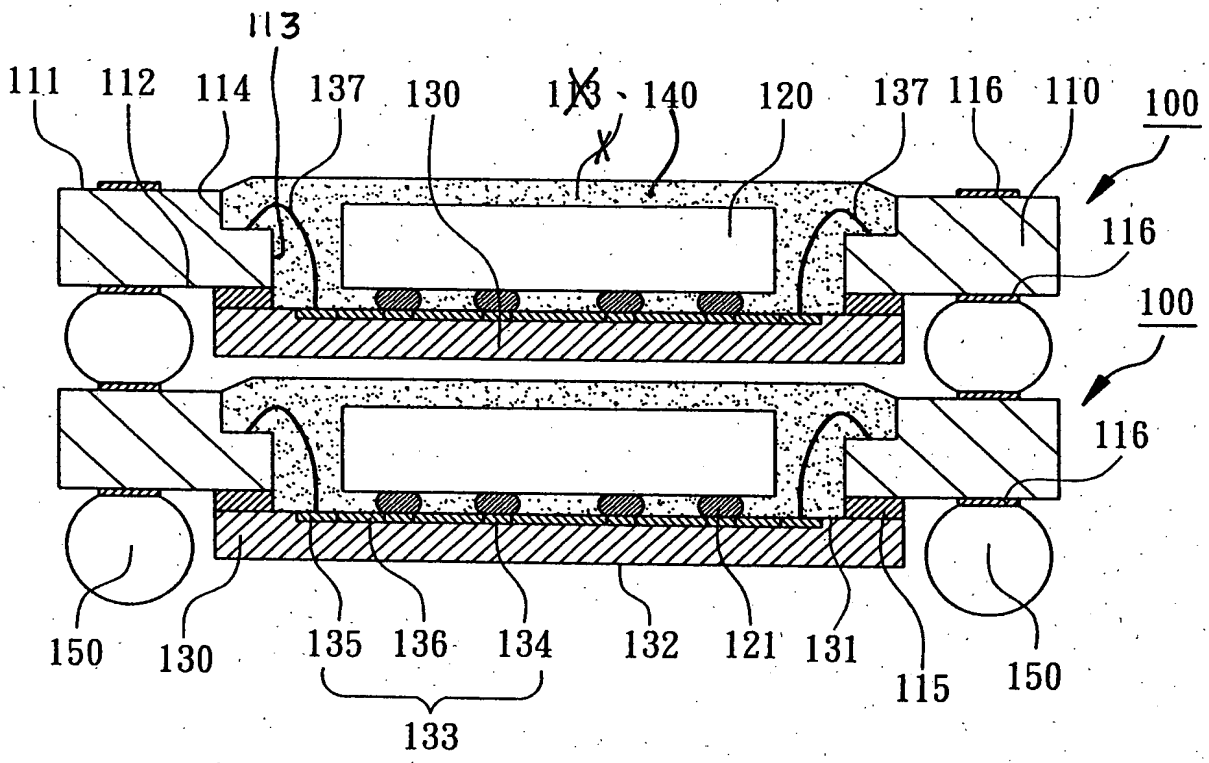

FIG. 3

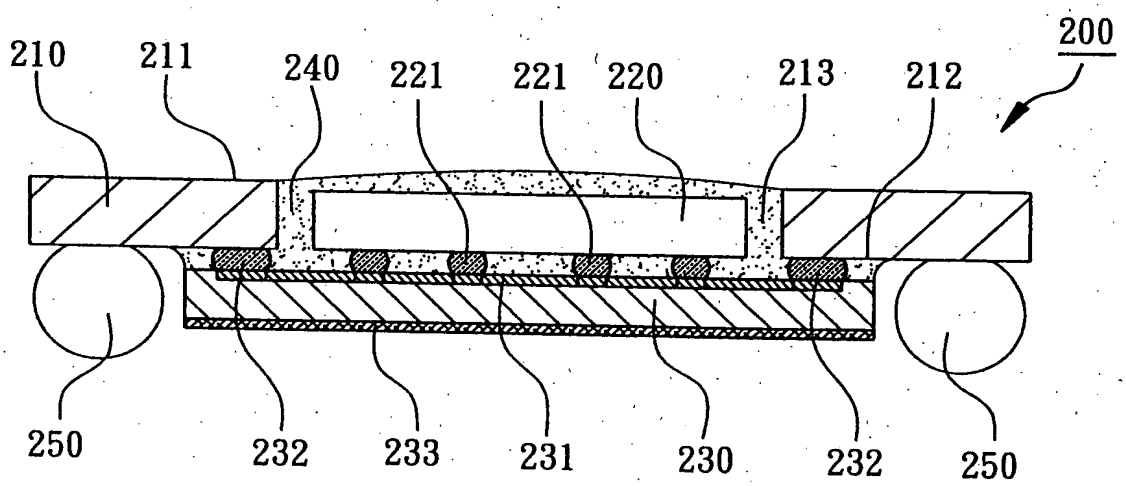

FIG. 4